The invention in which an exclusive right is claimed is defined by the following:

1. A method for prefetching data stored in a memory, comprising the steps of:

(a) providing a reference address associated with a machine instruction that is executable to carryout a function other than prefetching the data;

(b) determining that the reference address indicates a location within a prefetch region of the memory, said prefetch region being defined by compile-time information associated with a set of machine instructions for processing the data;

(c) determining an address of a prefetch block of the data within the prefetch region as a function of the reference address and the compile-time information; and

(d) prefetching the prefetch block of the data from the prefetch region of the memory before the prefetch block of the data are required for processing in accord with the set of machine instructions.

2. The method of Claim 1, wherein the step of determining that the reference address indicates a location within the prefetch region comprises one of the steps of:

(a) determining that the reference address indicates a location within a one-dimensional prefetch region of the memory; and

(b) determining that the reference address indicates a location within a multi-dimensional prefetch region of the memory.

3. The method of Claim 2, wherein the step of determining that the reference address indicates a location within the one-dimensional prefetch region comprises the steps of:

(a) accessing a base address included in the compile-time information, said base address identifying a beginning of a continuous segment of memory comprising the one-dimensional prefetch region;

(b) accessing a size included in the compile-time information, said size identifying an extent of the continuous segment of memory comprising the one-dimensional prefetch region; and

(c) determining that the reference address lies between the base address and a final address defined by a sum of the base address and the size.

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4. The method of Claim 2, wherein the step of determining that the reference address indicates a location within the multi-dimensional prefetch region of the memory comprises the steps of:

(a) accessing a base address and a size of the memory in at least one dimension that are included in the compile-time information, said base address identifying a beginning of an embedded portion of the memory comprising the multi-dimensional prefetch region;

(b) accessing an embedded size of each dimension of the multi-dimensional prefetch region included in the compile-time information, said embedded size of each dimension identifying an extent of the embedded portion of memory in the dimension of the multi-dimensional prefetch region;

(c) accessing a size for each dimension of a block of data to be prefetched; and

(d) determining that the reference address lies within the embedded portion of memory as a function of the base address and a final address corresponding to each embedded size of each dimension of the multi-dimensional prefetch region.

5. The method of Claim 1, wherein the step of determining the address of the prefetch block comprises one of the steps of:

(a) determining the address of the prefetch block within a one-dimensional prefetch region of the memory; and

(b) determining the address of the prefetch block within a multi-dimensional prefetch region of the memory.

6. The method of Claim 3, wherein the step of determining the address of the prefetch block comprises the steps of:

(a) accessing a prefetch size included in the compile-time information, said prefetch size identifying a size of the prefetch block;

(b) accessing a prefetch distance included in the compile-time information, said prefetch distance identifying an offset from the reference address to a location within the prefetch block; and

(c) determining a starting address of the prefetch block as a function of the reference address, the size, the prefetch size, and the prefetch distance.

7. The method of Claim 4, wherein the multi-dimensional prefetch region is a two-dimensional prefetch region; and wherein the step of determining the address of the prefetch block comprises the steps of:

(a) accessing a prefetch width included in the compile-time information, said prefetch width identifying a horizontal size of the prefetch block;

(b) accessing a prefetch height included in the compile-time information, said prefetch height identifying a vertical size of the prefetch block;

(c) accessing a width distance included in the compile-time information, said width distance identifying a horizontal distance to a location within the prefetch block, said horizontal distance being measured from a grid base address that is determined as a function of the reference address;

(d) accessing a height distance included in the compile-time information, said height distance identifying a vertical distance to a location within the prefetch block, said horizontal distance being measured from the grid base address; and

(e) determining a starting address of the prefetch block as a function of the reference address, the prefetch width, the prefetch height, the width distance, and the height distance.

8. The method of Claim 1, wherein the step of prefetching the prefetch block of the data comprises the step of conveying the prefetch block of the data to a cache.

9. The method of Claim 8, wherein the step of conveying the prefetch block of the data to a cache comprises the step of loading the prefetch block of the data into a prefetch buffer within the cache.

10. The method of Claim 9, further comprising the step of conveying the prefetch block of the data from the prefetch buffer to a data area of the cache for use by a processor.

11. The method of Claim 1, further comprising the step of determining that the prefetch block of the data is not already stored in a prefetch buffer of a cache used to temporarily store the data for use by a processor, prior to the step of prefetching the prefetch block of the data.

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12. The method of Claim 1, further comprising the step of determining that the prefetch block of the data is not already stored in a write buffer of a cache used to temporarily store the data for use by a processor, prior to the step of prefetching the prefetch block of the data.

13. The method of Claim 1, further comprising the step of determining that the prefetch block of the data is not already stored in a data area of a cache used to temporarily store the data for use by a processor, prior to the step of prefetching the prefetch block of the data.

14. A machine-readable medium having machine instructions for performing the steps of Claim 1.

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15. A system for program-directed prefetching of data for use by a media processor, comprising:

(a) a memory that stores data accessible by the media processor, said memory including a cache in which portions of the data are temporarily stored and are more rapidly accessed by the media processor for processing than the data stored in other portions of the memory; and

(b) a program-directed prefetch (PDP) controller in communication with the cache, said PDP controller providing the cache with compile-time information that defines a prefetch region of the memory and indicates prefetch data to be prefetched from the prefetch region of the memory in response to a program instruction that is included to cause the media processor to carryout a function other than prefetching data.

16. The system of Claim 15, wherein the PDP controller comprises a set of registers that stores the compile-time information defining the prefetch region of the memory.

17. The system of Claim 15, wherein the PDP controller provides compile-time information for one of:

(a) one-dimensional prefetching, wherein the one-dimensional prefetching accesses prefetch data from a continuous segment of the memory comprising the prefetch region; and

(b) multi-dimensional prefetching, wherein the multi-dimensional prefetching accesses prefetch data from an embedded segment of the memory comprising a multi-dimensional prefetch region.

18. The system of Claim 17, wherein the compile-time information for the one-dimensional prefetching comprises:

(a) a base address of a one-dimensional prefetch region in the memory;

(b) a size defining a continuous extent of the one-dimensional prefetch region in the memory;

(c) a prefetch size indicating a block size of data to be prefetched;

(d) a distance to a location of a desired block of data to be prefetched, said distance being measured from a machine instruction reference address lying within the prefetch region; and

(e) a mode indicating a mode of a prefetching operation.

19. The system of Claim 17, wherein the compile-time information for multi-dimensional prefetching comprises:

(a) a base address of the multi-dimensional prefetch region in the memory and a size of the memory in at least one dimension;

(b) a size for each dimension of the multi-dimensional prefetch region;

(c) a size for each dimension of a block of data to be prefetched;

(d) a distance in each dimension to a location of the block of data to be prefetched, each distance being measured from a grid base address that is a function of a reference address for the program instruction lying within the multi-dimensional prefetch region; and

(e) a mode indicating a mode of prefetching operation.

20. The system of Claim 15, wherein the cache comprises:

(a) a cache controller in communication with the PDP controller, said cache controller utilizing the compile-time information to prefetch data from the prefetch region of the memory; and

(b) a prefetch buffer for storing data prefetched from the prefetch region of the memory.

21. The system of Claim 20, said cache further comprising a data area in communication with the cache controller and the prefetch buffer, said cache controller causing prefetched data stored in the prefetch buffer to be conveyed to the data area for use by the media processor.

22. The system of Claim 21, wherein the data area comprises the prefetch buffer.

23. The system of Claim 15, wherein the PDP controller is in communication with the media processor and receives a reference address from the media processor, said reference address identifying a location in the prefetch region of the memory from which the prefetch data are offset.

24. A media processor for prefetching media data stored in a memory to avoid programming a direct memory access function to access the media data, comprising:

(a) a function unit that executes machine instructions;

(b) a cache in communication with the function unit, said cache temporarily storing portions of the media data for use by the function unit in executing the machine instructions; and

(c) a program-directed prefetch (PDP) controller in communication with the function unit and the cache, said PDP controller storing compile-time information that defines a prefetch region of the memory and defines an offset to a prefetch block of the media data in the memory, said prefetch block of the media data being prefetched from a location in the memory determined as a function of the offset and as a function of a reference address indicated by a machine instruction that is executed by the function unit for a purpose other than prefetching data.

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25. The media processor of Claim 24, wherein the PDP controller comprises a set of registers in which the compile-time information is stored.

26. The media processor of Claim 24, wherein said prefetch block of the media data is prefetched by one of:

(a) one-dimensional prefetching, wherein one-dimensional prefetching accesses prefetch data from a continuous segment of the memory comprising the prefetch region; and

(b) multi-dimensional prefetching, wherein multi-dimensional prefetching accesses prefetch data from an embedded segment of the memory comprising the prefetch region.

27. The media processor of Claim 26, wherein the compile-time information for one-dimensional prefetching comprises:

(a) a base address of the continuous segment of the memory comprising the prefetch region;

(b) a size defining an extent of the continuous segment of the memory comprising the prefetch region;

(c) a prefetch size indicating a block size of data to be prefetched from the continuous segment of the memory comprising the prefetch region;

(d) a prefetch distance indicating a distance to a location of a desired block of data to be prefetched, said distance being measured from the reference address within the prefetch region indicated by the machine instruction; and

(e) a mode indicating a mode of prefetching operation.

28. The media processor of Claim 26, wherein the multi-dimensional prefetch region is a two-dimensional prefetch region; and wherein the compile-time information for two-dimensional prefetching comprises:

(a) a base address of the embedded segment of the memory comprising the prefetch region;

(b) a pitch indicating an extent of continuous media data stored in the memory corresponding to a horizontal dimension of an image;

(c) a width indicating an extent of the media data stored in the memory and corresponding to a partial length of the horizontal dimension of the image, said width further indicating a horizontal dimension of the embedded segment of the memory comprising the prefetch region;

(d) a height indicating an extent of continuous media data stored in the memory corresponding to a vertical dimension of the image;

(e) a prefetch width indicating a horizontal size of a block of data to be prefetched;

(f) a prefetch height indicating a vertical size of the block of data to be prefetched;

(g) a prefetch width distance indicating a horizontal distance to a location of the block of data to be prefetched, said horizontal distance being measured from a grid base address that is a function of said reference address within the embedded segment;

(h) a prefetch height distance indicating a vertical distance to the location of the block of data to be prefetched, said vertical distance measured from the grid base address that is a function of said reference address within the embedded segment; and

(i) a mode indicating a mode of prefetching operation.

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29. The media processor of Claim 24, wherein the cache comprises:

(a) a cache controller in communication with the PDP controller and the function unit, said cache controller utilizing the compile-time information to prefetch media data from the prefetch region of the memory; and

(b) a prefetch buffer for storing media data prefetched from the prefetch region of the memory.

30. The media processor of Claim 29, further comprising a data area in communication with the cache controller and prefetch buffer, said cache controller causing prefetched media data stored in the prefetch buffer to be communicated to the data area for use by the media processor.

31. The media processor of Claim 30, wherein the data area comprises the prefetch buffer.

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